

IN THE UNITED STATES
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PATENT APPLICATION

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CASE 2-2

TITLE An Integrated Circuit Carrier And Method Of Manufacturing

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification

4 Informal sheets of drawing(s)

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	20 - 20 =	0	x \$22 =	\$0
Independent Claims	5 - 3 =	2	x \$82 =	\$164
Multiple Dependent Claim(s), if applicable			\$270 =	\$0
Basic Fee				\$790
TOTAL FEE:				\$954

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Respectfully,

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Date: August 21, 1998
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AN INTEGRATED CIRCUIT CARRIER AND METHOD OF MANUFACTURING AND INTERGRATED CIRCUIT

Cross-Reference To Related Application

This application claims priority of Provisional Application Serial No.
5 60/095397 which was filed on August 5, 1998 (Lucent Attorney Docket No.
M. B. Baillie 2-2).

Field of the Invention

The present invention relates generally to a process of integrated circuit
manufacture and electronic devices and, particularly, to process for using a carrier tape to
10 manufacture integrated circuits and electronic devices.

Background of the Invention

There has been an increasing demand to improve the efficiency of
manufacturing integrated circuits and electronic devices. One method for improving
efficiency is using carrier tape packages to automate the manufacturing process. Fig. 4 is
15 a schematic diagram of a carrier tape 400 holding a number of integrated circuits 410
positioned in a chip carrier 420. The carrier tape 400 is used to transport the integrated
circuits 410 and allow the integrated circuits 410 to be retrieved from the carrier using
automated manufacturing equipment. For example, the carrier tape 400 may be fed to an
apparatus which retrieves the integrated circuits from the carrier tape and populates a
20 circuit board.

Fig. 5 is a schematic diagram along line 5-5 of the chip carrier 420 for
holding an integrated circuit 410 in a carrier tape 400 according to the prior art. The chip
carrier 420 includes a base 520 for receiving an integrated circuit 410. A well 530 is
formed around the base 520. An integrated circuit is held in the chip carrier 420 by a
25 cover 540 which is attached to the upper surface 510 by an adhesive. The integrated
circuit 410 disposed in the chip carrier 420 may be damaged if force from, for example,

an impact is applied to the wall 532. The leads of the integrated circuit 410 may be damaged from such an impact. In addition, the chip carrier 420 may be susceptible to impacts on the bottom 520 of the chip carrier 420. As a result, it is desirable to provide a chip carrier which reduces the potential damaged to an integrated circuit disposed in the chip carrier.

Summary of the Invention

The present invention provides a process of manufacturing an integrated circuit. The process includes the steps of providing a chip carrier including a base, an inner well formed about the periphery of the base, and an outer well formed about the periphery of the inner well. An integrated circuit is positioned on the base. The process further includes the steps of pre or post processing the integrated circuit.

The present invention is also directed to a process of transporting an integrated circuit using a chip carrier including a base, an inner well formed about the periphery of the base, and an outer well formed about the periphery of the inner well.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

Brief Description of the Drawing

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice in the semiconductor industry, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a schematic diagram of a chip carrier according to an illustrative embodiment of the present invention;

Fig. 2 is a top view of the chip carrier shown in Fig. 1;

Fig. 3 is a flow chart diagram for manufacturing an electronic device;

Fig. 4 is a top view of a carrier tape according to the prior art; and

Fig. 5 is a cross sectional view along line 5-5 of the carrier tape shown in Fig. 4.

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Detailed Description of the Invention

The illustrative embodiment of the present invention provides a chip carrier that includes a double well structure including an inner well and an outer well. The double well structure forms a flexible structure that adsorbs the force generated by impacts. In addition, the outer well is deeper than the inner well to provide crush protection from bottom side impacts. As a result, a device positioned in the chip carrier may be protected from damage.

Referring now to the drawing, wherein like reference numerals refer to like elements throughout, Fig. 1 is a schematic diagram of a chip carrier 100 according to an illustrative embodiment of the present invention. The chip carrier 100 includes an upper service 110 and a base 115. Adjacent to and disposed around the base 115 is an inner well 120. An outer well 125 is positioned adjacent to and disposed around the inner well 120. The walls 130, 134, and 136 of the inner well 120 and the outer well 125 form an S-shape.

The outer well 125 includes a first wall 130 extending from the upper surface 110 towards a first position 132 and a second wall 134 extending from the first position 132 towards a reference plane 135 defined by the upper surface 110. The inner well 120 includes a third wall 136 extending away from the reference plane towards a second position 138 and a fourth wall 140 extending away from the second position 138. A cover 160 is fixed to the upper surface 110 to hold the integrated circuit 150 in the chip carrier 100. The cover 160 is attached to the upper surface 110 by, for example, an adhesive.

Figure 2 is a top view of the chip carrier 100 along line 2-2. The bottom of the inner well 120 and the bottom of the outer well 125 are identified by cross hatching. The cover 160 of the chip carrier 160 has been removed for clarity. The inner well 120 and the outer well 125 may or may not be continuous. For example, the inner and outer wells may be continuously formed to protect the leads of an integrated circuit having leads formed on four sides (e.g., a quad flat pack). Alternatively, if the integrated circuit includes leads on two sides, the inner and out wells may be formed adjacent to the leads and not adjacent to the other sides that do not contain leads.

The outer well 125 and the inner well 120 protect an integrated circuit 150 positioned on the base 115 from impacts to the chip carrier 100 on the wall 130. During a side impact, the walls 130, 134, and 136 move absorbing the force of the impact and preventing lead damage. In other words, the S-shape of the walls compresses absorbing the force of side impacts. In addition, the outer well 125 is slightly deeper than the inner well 120 in the y-direction. In other words, the outer well 125 extends farther away from the upper surface 110 than the inner well 120. As a result, the outer well 125 protects an integrated circuit from damage caused by impacts on the bottom of the chip carrier 100. For example, an object impacting the chip carrier 100 contacts the outer well 125 which absorbs the impact without transferring the impact energy to the integrated circuit 150. Accordingly, large integrated circuits with fragile leads such as quad flat pack packages (e.g., MQFP, SQFP, and TQFP packages) may be shipped using tape and reel packed shipment.

In an illustrative embodiment, the base 115 extends a distance D1 of .059 inches below the upper surface 110. The second position 138 extends a distance D2 of .094 inches below the upper surface 110. The first position 132 extends a distance D3 of .107 inches from the upper surface 110. The position 139 between the inner well 120 and the outer well 125 extends a distance D4 of .011 inches from the upper surface 110. Distance D4 may range from .005 inches to .025 inches, depending on the desired flexibility. The chip carrier may be constructed from polycarbonate resin, polystyrene resin, PVC resin, or PET (polyethylene) resin. Carrier tapes may require ESD protection in the form of carbon coating or filling of the tape. The thickness or width W of the material from which the material for the tape carrier 100 is embossed, drawn, or vacuum formed is

usually in the range of .010 inches to .015 inches. Some sections of the carrier tape following the forming operation may be as thin as .006 inches.

Fig. 3 is directed to another exemplary embodiment of the present invention using the chip carrier shown in Figs. 1 and 2. At step 400, an integrated circuit is manufactured. The process for manufacturing an integrated circuit is described in Silicon Processing for the VLSI Era, Vols. 1-3 by Stanley Wolf, Lattice Press (1990). At step 405, the integrated circuit is placed on the base 115 (shown in Fig. 1) using, for example, an automated transfer device (not shown). At step 410, the cover is affixed to the upper service 110 of the chip carrier 100 to hold the integrated circuit in position. At step 415, the chip carrier 100 is transported. For example, the chip carrier 100 may be transported for use in another manufacturing tool located in the same facilities where the integrated circuit was manufactured. Alternatively, the chip carrier 100 may be transported to another physical location. The chip carrier 100 may be transferred by automated equipment, airplane, truck, and/or other transportation systems, alone or in combination. At step 420, the integrated circuit is removed from the chip carrier 100 for further processing. The further processing may include additional manufacturing processes to complete the integrated circuit. Alternatively, the integrated circuit may be used to populate a circuit board as is well-known in the art. In addition, the integrated circuit may be used in the manufacture of other electronic equipment.

Although the invention has been described with reference to exemplary embodiments, it is not limited to those embodiments. Rather, the appended claims should be construed to include other variants and embodiments of the invention which may be made by those skilled in the art without departing from the true spirit and scope of the present invention.

What is Claimed:

- 1 1. A chip carrier comprising:
2 a base,
3 an inner well formed about the periphery of the base; and
4 an outer well formed about the periphery of the inner well.
- 1 2. The chip carrier according to claim 1 wherein the first well and the
2 second well form a flexible structure.
- 1 3. The chip carrier according to claim 1 wherein the outer well
2 includes an outer wall and an inner wall and the inner well includes an outer wall coupled
3 to the inner wall of the outer well.
- 1 4. The chip carrier according to claim 1 further comprising an upper
2 surface and wherein the outer well extends farther away from the upper surface than the
3 inner well.
- 1 5. The chip carrier according to claim 1 further comprising an
2 integrated circuit positioned on the base.
- 1 6. The chip carrier according to claim 1 wherein the outer well and
2 the inner well are continuous.
- 1 7. The chip carrier according to claim 1 wherein at least one of the
2 outer well and the inner well are not continuous.
- 1 8. A process of manufacturing an integrated circuit comprising:
2 providing the integrated circuit;
3 providing a chip carrier including a base, an inner well formed about the
4 periphery of the base, and an outer well formed about the periphery of the inner well; and
5 positioning the integrated circuit on the base.
- 1 9. The process of claim 8 further comprising sealing the integrated
2 circuit in the chip carrier.
- 1 10. The process of claim 9 further comprising providing the chip
2 carrier with a continuous outer well.

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1 18. The carrier according to claim 17 wherein the third wall and the
2 fourth wall form a second well.

1 19. The carrier according to claim 14 wherein the third wall and the
2 fourth wall form a well.

1 20. A method of transporting a device comprising:
2 providing a carrier including a base, an inner well formed about the
3 periphery of the base, and an outer well formed about the periphery of the inner well; and
4 moving the device from a first location to a second location in the carrier

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AN INTEGRATED CIRCUIT CARRIER AND METHOD OF MANUFACTURING AND INTERGRATED CIRCUIT

ABSTRACT

A process for manufacturing an integrated circuit including the steps of providing a chip carrier including a base, an inner well formed about the periphery of the base, and an outer well formed about the periphery of the inner well. An integrated circuit is positioned on the base. The process further includes the steps of pre or post processing the integrated circuit.

Fig. 1

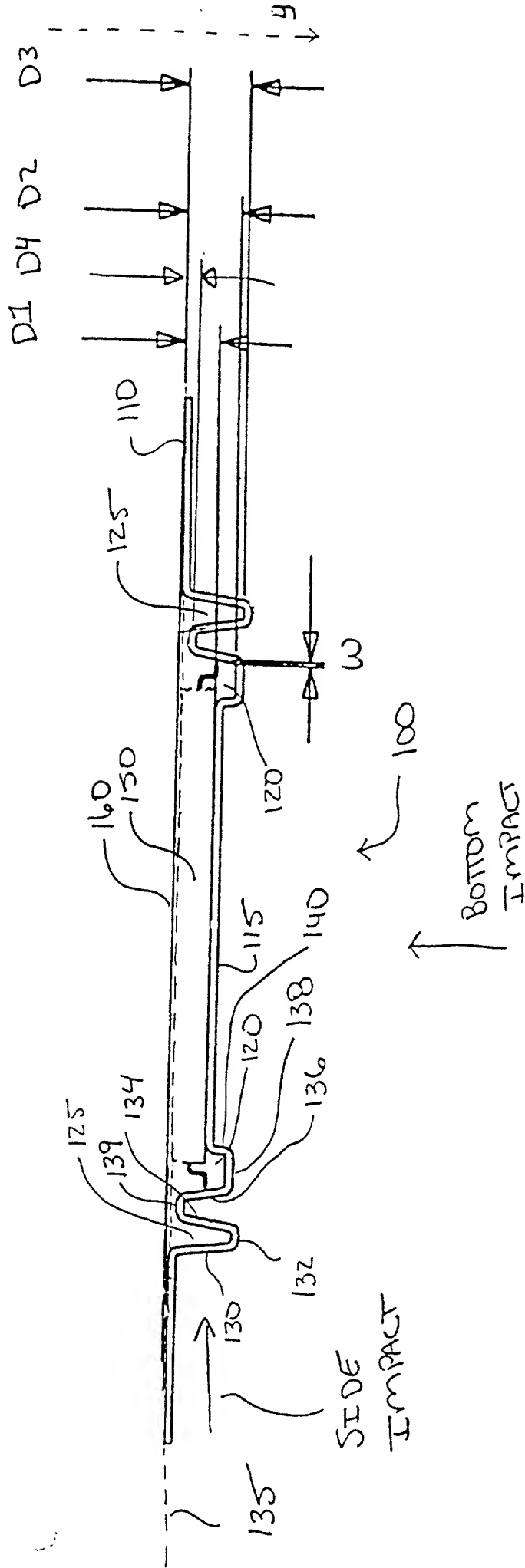


Fig. 2

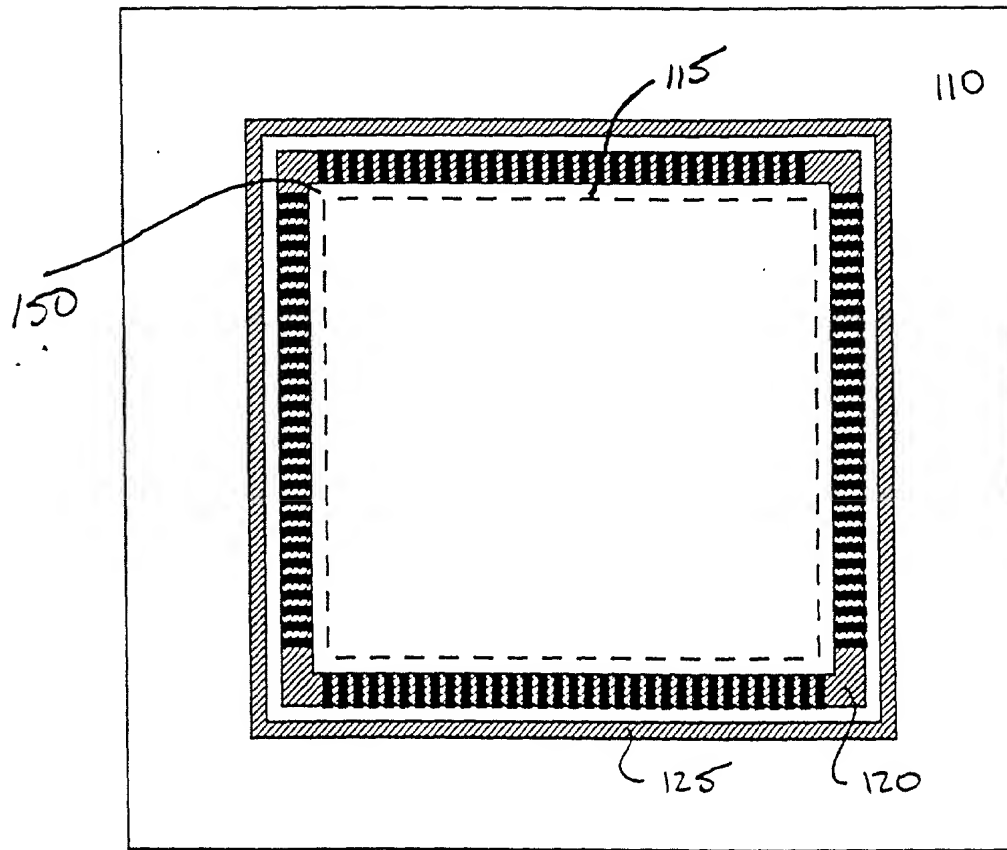
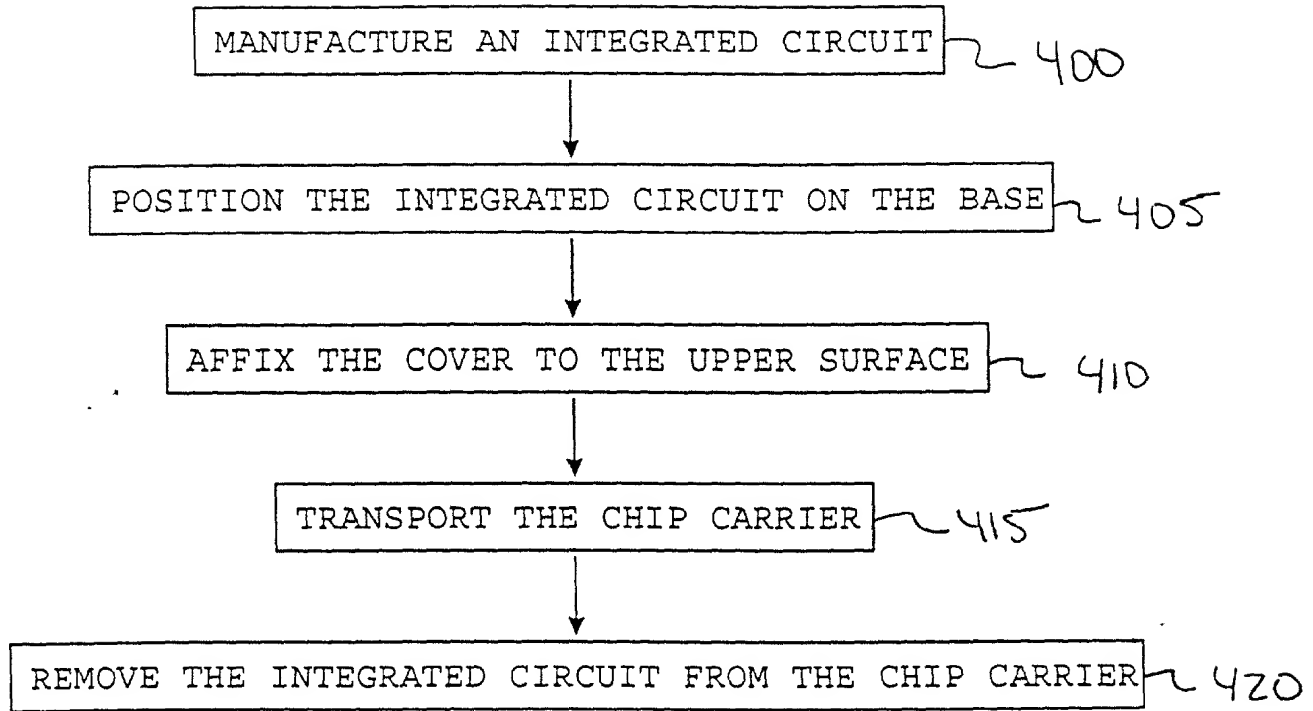


Fig. 3



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Fig. 4

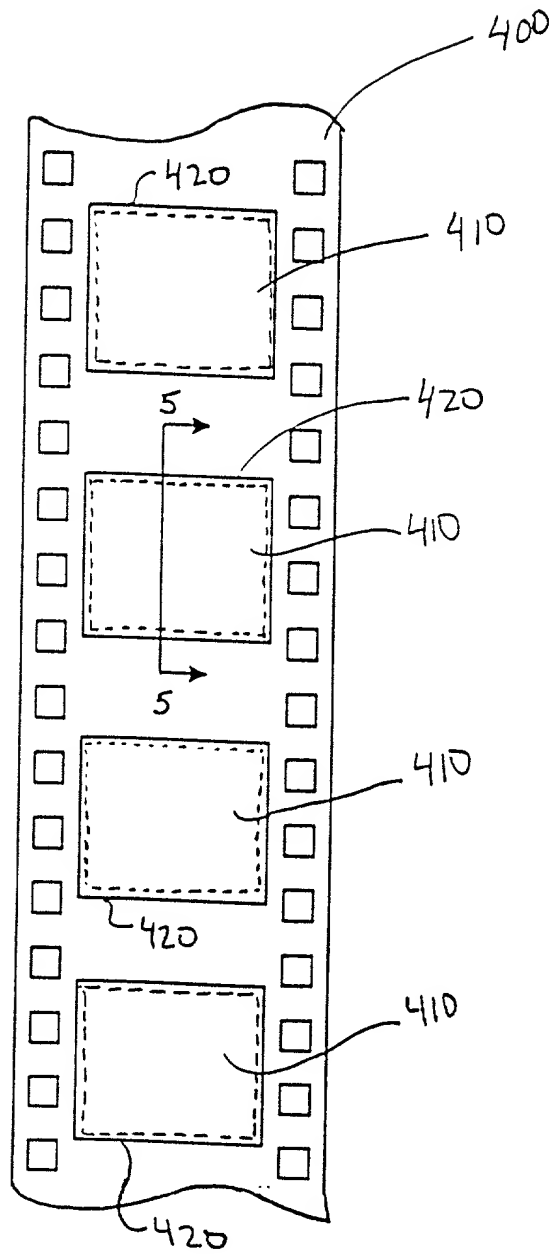
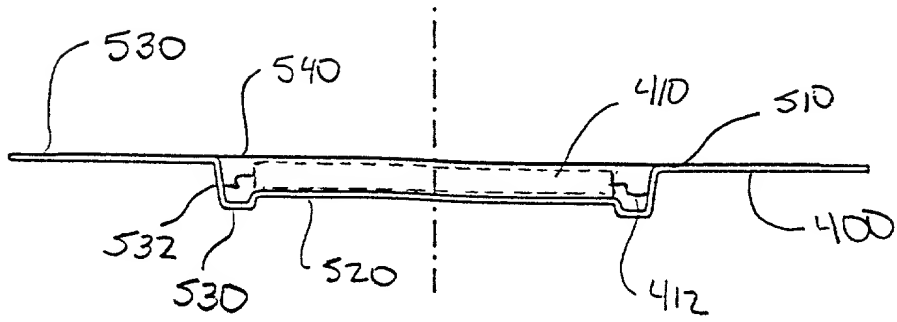
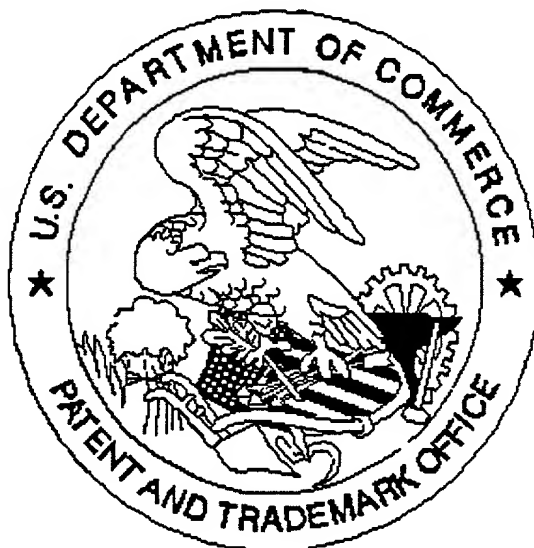


Fig. 5



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